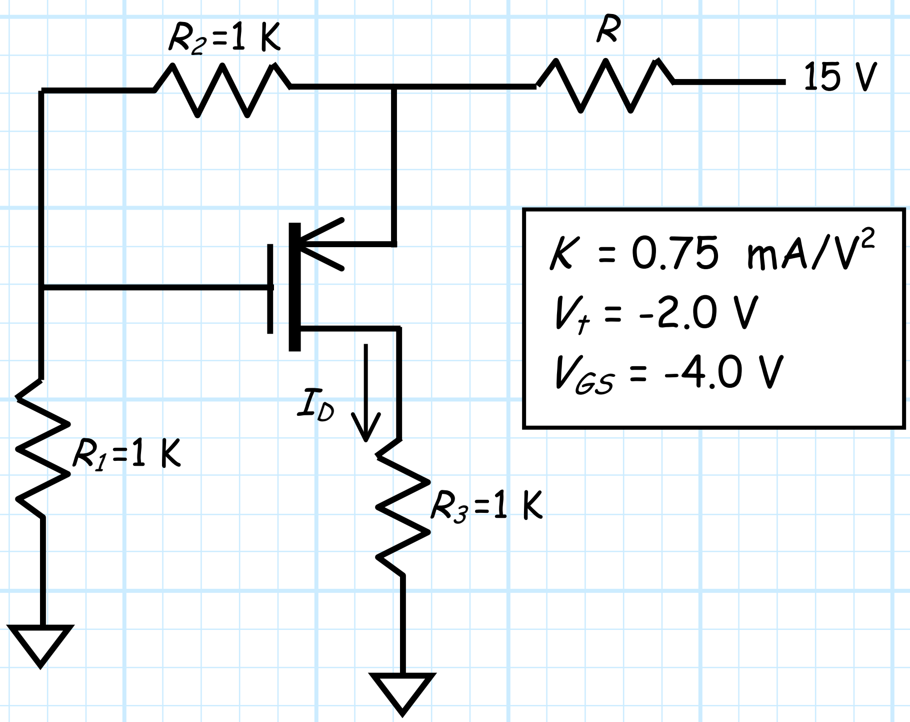
Example: Another PMOS Circuit Analysis

Consider the **PMOS** circuit below, where we know (somehow) that V_{GS} = -4.0 V, but don't know (for some reason) the value of resistor *R*.

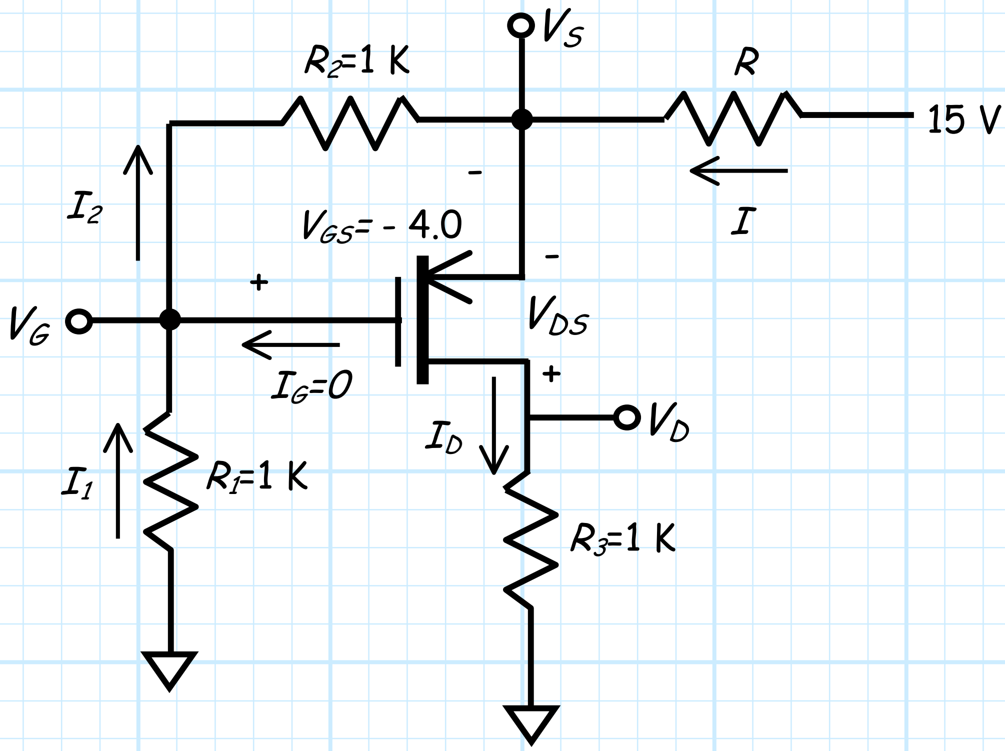


Let's see if we can determine the value of resistor *R*.

First, let's ASSUME that the MOSFET is in saturation, and therefore ENFORCE the drain current equation:

$$I_D = K\left(V_{GS} - V_t\right)^2$$

Now we ANALYZE the circuit:



Since we know that V_{GS}=-4.0 V, and we ASSUMED that the PMOS device was in saturation, we can directly determine the drain current I_D:

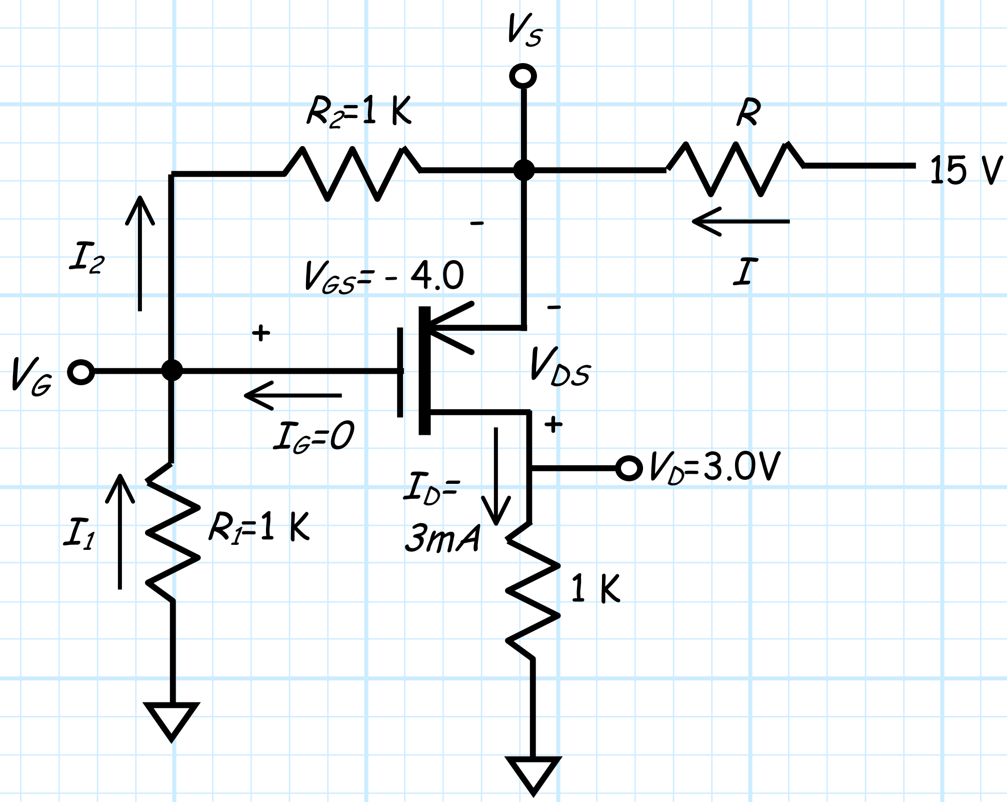
$$\begin{aligned} I_D &= K\left(V_{GS} - V_t\right)^2 \\ &= 0.75\left(-4.0 - (-2.0)\right)^2 \\ &= 0.75\left(-4.0 + 2.0\right)^2 \\ &= 3\, mA \end{aligned}$$

and thus the drain voltage V_D is:

$$\begin{aligned} V_D &= 0.0 + I_D R_3 \\ &= 0.0 + (3.0)1.0 \\ &= 3.0 \text{ V} \end{aligned}$$

Q: *OK, this first part was easy, but what do we do now? How can we determine the value of resistor R ?*

A: The key to "unlocking" this circuit analysis is recognizing that the potential difference across resistor R_2 is simply the voltage V_{GS}—and we **know** the value of V_{GS} (V_{GS} =-4.0V)!



Thus, we can immediately determine that current I_2 is:

$$I_2 = \frac{V_{GS}}{R_2} = \frac{-4.0}{1} = -4.0\ mA$$

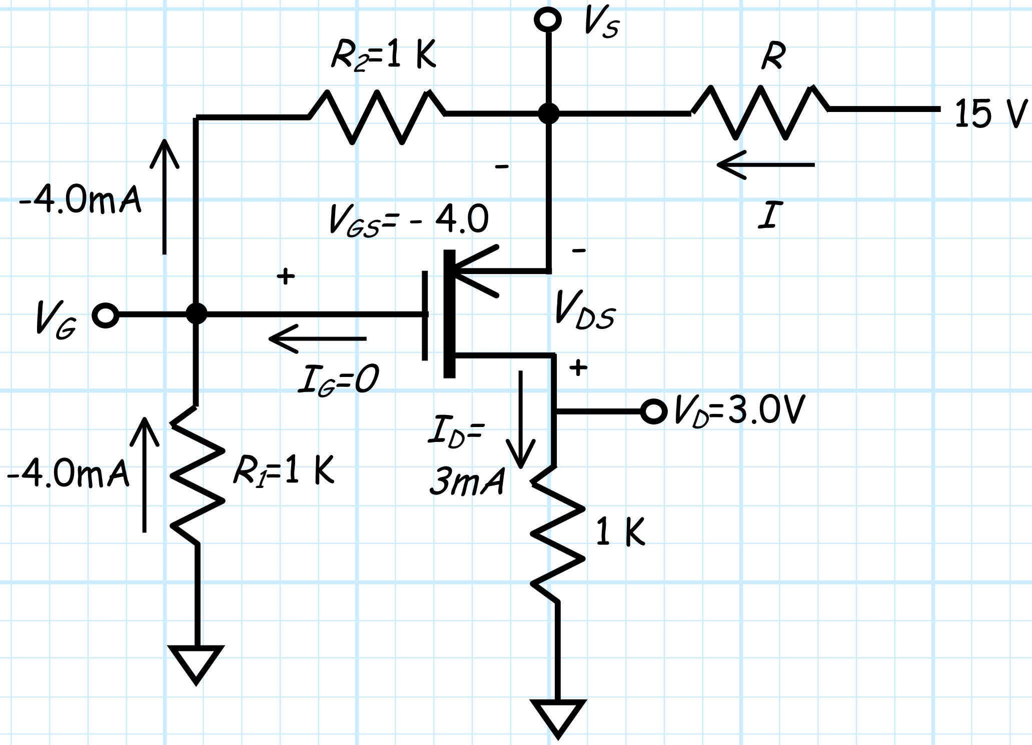
Likewise, from KCL, we find:

$$I_1 + I_G = I_2$$

But since gate current $I_G = 0$, we conclude:

$$I_1 = I_2 = -4.0 \; mA$$

Now we can determine much about this circuit!

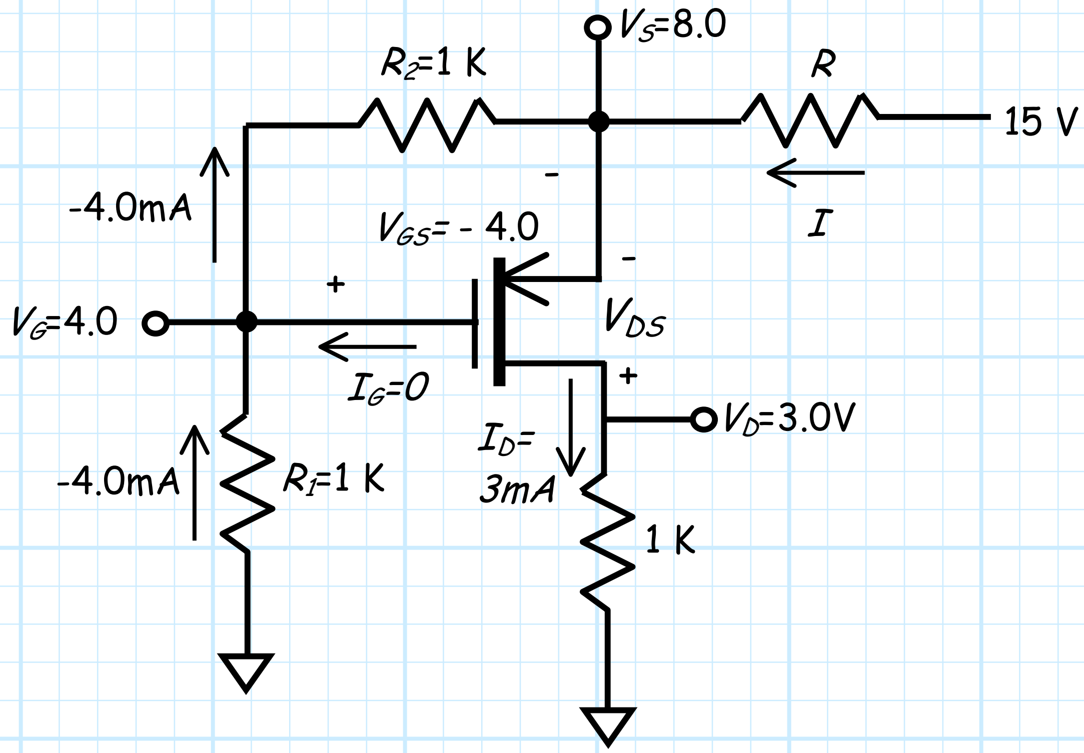


For example, from KVL, we find the gate voltage:

$$\begin{aligned} V_G &= 0.0 - I_1 R_1 \\ &= -(-4.0)1 \\ &= 4.0 \text{ V} \end{aligned}$$

And likewise the source voltage:

$$\begin{aligned} V_S &= V_G - I_2 R_2 \\ &= 4.0 - (-4.0)1 \\ &= 8.0 \text{ V} \end{aligned}$$



Likewise, from KCL, we can determine the current through resistor R:

$$\begin{aligned} I &= I_D - I_2 \\ &= 3.0 - (-4.0) \\ &= 7.0\ mA \end{aligned}$$

And thus from Ohm's Law we can find the value of R:

$$\begin{aligned} R &= \frac{15.0 - V_S}{I} \\ &= \frac{15.0 - 8.0}{7.0} \\ &= 1\ K \end{aligned}$$

But wait! We're still not done! We must CHECK to see if our original ASSUMPTION was correct.

First, we CHECK to see if the channel is induced:

$$V_{GS} = -4.0 < -2.0 = V_t \quad \checkmark$$

Next, we CHECK to see if the channel is pinched off. Here, we note that $V_{DS} = V_D - V_S = 3.0 - 8.0 = -5.0 \text{ V}$, and excess gate voltage is $V_{GS} - V_t = -4.0 - (-2.0) = -2.0 \text{ V}$. Therefore:

$$V_{DS} = -5.0 < -2.0 = V_{GS} - V_t \quad \checkmark$$

Hence, our ASSUMPTION is correct, and $R = 1\text{K}$.